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# Ceramic Column Grid Array Design and Manufacturing Rules for Flight Hardware

**February 22, 2011**

The latest version of this standard is located at the GSFC Standards website at
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# DOCUMENT HISTORY LOG

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# FOREWORD

This standard is published by the Goddard Space Flight Center (GSFC) to provide uniform engineering and technical requirements for processes, procedures, practices, and methods that have been endorsed as standard for NASA programs and projects, including requirements for selection, application, and design criteria of an item.

This standard establishes requirements which apply to all uses on flight hardware of ceramic-packaged electronic parts which are solder-attached to printed circuit boards with solder columns (ceramic column grid array attachments or CCGAs). The requirements address as-received part inspection, printed circuit board design, manufacturing process and quality control, process inspection points, inspection techniques and associated inspection criteria, rework, and process control validation testing. These requirements do not address subassembly-level design qualification.

Requests for information, corrections, or additions to this standard should be submitted via "Feedback" in the GSFC Technical Standards System at https://standards.gsfc.nasa.gov.

**In this document, a requirement is identified by "shall," a good practice by "should," permission by "may" or "can," expectation by "will," and descriptive material by "is."**

*Approval by:*

*Original signed by:*

George Alcorn
**GSFC Technical Standards Coordinator**

*Original signed by:*

Steven Scott
**GSFC Chief Engineer**

*Concurrence by:*

*Original signed by:*

Judith Bruner
**Director of Safety and Mission Assurance**

*Original signed by:*

Dennis Andrucyk
**Director of Applied Engineering and Technology**

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# Ceramic Column Grid Array Design and Manufacturing Rules for Flight Hardware

## 1.0 SCOPE

### 1.1 Purpose

The purpose of this standard is to provide requirements and recommendations intended to facilitate production of defect-free ceramic column grid array solder joint interconnects to boards intended for use in space flight applications (refer to Appendix A, Technology Background). This standard does not provide application specific reliability test requirements (e.g. qualification requirements).

### 1.2 Applicability

This standard is applicable to all uses on flight hardware of ceramic packaged electronic parts which are solder-attached to printed circuit boards with solder columns (ceramic column grid array attachments or CCGAs).

## 2.0 APPLICABLE DOCUMENTS

### 2.1 General

The documents listed in this section contain provisions that constitute requirements of this standard as cited in the text of Section 4.0, Requirements. The latest issuances of cited documents shall be used unless otherwise approved by the assigned Technical Authority. The applicable documents are accessible via the NASA Technical Standards System at http://standards.nasa.gov, directly from the Standards Developing Organizations, or from other document distributors.

### 2.2 Government Documents

| | |
|---|---|
| IPC J-STD-001xS | Space Applications Electronic Hardware Addendum to J-STD-001x Requirements for Soldered Electrical and Electronic Assemblies* |
| MIL-STD-883 | Test Method for Microcircuits, Method 2009 |
| NASA-STD-8739.1A | Workmanship Standard for Polymeric Application on Electronic Assemblies |
| NASA-STD-8739.2 | Surface Mount Technology |
| NPD 8730.2 | NASA Parts Policy |

* The “x” in the document number is a placeholder for the revision letter.

### 2.3 Non-Government Documents

| | |
|---|---|
| AS9100 | Quality Management Systems – Aerospace - Requirements |
| IPC-6012 | Qualification and Performance Specification for Rigid Printed Boards |
| IPC- 9701 | Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments |
| IPC-TM-650 | Test Method for Bow and Twist (Percentage) |

### 2.4 Order of Precedence

When this standard is applied as a requirement or imposed by contract on a GSFC program or GSFC project, the technical requirements of this standard take precedence, in the case of conflict, over the technical requirements cited in applicable documents or referenced guidance documents.

## 3.0 ACRONYMS AND DEFINITIONS

### 3.1 Acronyms/Definitions

CGA – Column Grid Array – Surface mount packaging that utilizes a grid pattern of solder columns as interconnects to the printed wiring board.

CCGA – Ceramic Column Grid Arrays – CGAs specifically using ceramic body packaging.

CM – Configuration Management

CTE – Coefficient of Thermal Expansion – Changes in volume of a material as a function of changes in temperature

ENIG – Electroless Nickel Immersion Gold

ESD – Electrostatic Discharge

FPGA – Field Programmable Gate Array – A programmable part which is used for data processing. Typical spaceflight packaging for this part consists of gull wing type leads on the sides of the package; however, current designs are using CCGA packaging.

I/O – Input/Output

LGA – Land Grid Array

PDL – Product Design Lead

PR/PFR – Problem Report/Problem Failure Report

PWA – Printed Wiring Assembly – A printed wiring board populated with parts.

PWB – Printed Wiring Board

QTP – Qualification Test Plan

SMT – Surface Mount Technology – A method of mounting electronic parts directly to the surface of a printed wiring board, instead of using through-hole technology. This method is commonly used in today's printed wiring assemblies.

# 4.0 REQUIREMENTS

## 4.1 Manufacturing and Quality Control Processes

Manufacturing and quality control processes shall be established as a minimum for:

a. Solder reflow equipment temperature, calibration and reflow profile configuration management (CM) control
b. Parts, materials and board storage and handling
c. Contamination control
d. Solder paste deposition methods and quality control
e. Part placement quality control
f. Proper selection and use of inspection equipment
g. Failure root cause investigation and corrective action

## 4.2 Incoming Parts Inspections

### 4.2.1 Parts Approval

All CCGA parts shall meet GSFC project specific mission assurance requirements for part selection and approval prior to use in flight hardware.

### 4.2.2 Part/Column Design

The package, solder, column materials, and number of columns shall be identified and documented on the assembly drawing and/or parts list. This information will be required for mechanical analysis and radiographic inspections. Table 1 lists typical materials.

***Reliability Note 4.1:*** The further the pins are from the package center point, or neutral point, the greater the thermally induced stress is on the solder joint; therefore parts with fewer columns are preferred.

**Table 1. Typical CCGA Package Designs**

| Package Body Material | Column Material | Package-to-Column solder | Column Size (h x d, mm) | Column Pitch (mm) |
|---|---|---|---|---|
| Ceramic | Pb90Sn10 (IBM type) | Eutectic tin-lead solder | 1.62 x 0.89 | 1.27 |
| Ceramic | Pb90Sn10 (IBM type) | Eutectic tin-lead solder | 2.21 x 0.51 | 1.27 |
| Ceramic | Pb80Sn20, Sn-plated Cu wrap, Sn63Pb37 finish (Six-Sigma type) | Eutectic tin lead solder | 2.21 x 0.51 | 1.27 |
| Ceramic | Pb80Sn20, Sn-plated Cu wrap, Sn63Pb37 finish (Six-Sigma type) | Eutectic tin lead solder | 2.21 x 0.51 | 1.00 |

### 4.2.3 Visual Inspection

All CCGA packages and columns shall be inspected prior to installation. Ten times (10X) magnification shall be used to establish that the parts comply with the following criteria:

a. No defects in the part body as defined in MIL-STD-883, Method 2009.
b. Package to column solder joint meets NASA-STD-8739.2 Paragraphs 12.8.2 (b) (1) through 12.8.2 (b) (15) requirements.
c. Solder fillet is present 100% around the circumference of the column.
d. For columns made with solder dipped copper wrap (copper reinforced columns) there shall be complete solder coverage on the entire column.
e. Columns shall appear uniform with no indication of bending or tilting.
f. All column locations and dimensions shall comply with the device manufacturer's drawing.

### 4.2.4 Column Coplanarity

Suppliers shall establish requirements for coplanarity and provide objective evidence to the GSFC project that it produces reliable hardware.

***Reliability Note 4.2:*** Part vendor guidelines circa 2010 specify co-planarity of the columns to be ±0.15 mm (±0.0059 in) or better, as measured from the worst case column to reference plane to ensure high quality CCGA attachments. It is strongly recommended that this value be imposed on the purchasing documentation (e.g. purchase order or source control drawing).

### 4.2.5 Solder Mask Inspection

Boards shall be 100% inspected at 10X magnification prior to use for any solder mask damage within the CCGA package pattern.

### 4.2.6 CCGA Land Area Inspection

Boards shall be 100% inspected prior to use for any pad damage within the CCGA package pattern.

### 4.2.7 Use of Units Rejected during Screening

A part (PWB or CCGA) that is found to be defective per the screening criteria in Sections 4.2.3, Visual Inspection, through 4.2.6, CCGA Land Area Inspection, requires review and approval by the GSFC project via its Material Review Board (MRB) process prior to its use.

## 4.3 PRINTED CIRCUIT BOARD DESIGN

### 4.3.1 Mechanical Design Analysis and Design Approval

Mechanical analysis shall be performed to verify that the designed part placement, board design, and board retention system will not overstress high quality CCGA solder joints over mission environmental conditions. The mechanical analysis shall address solder joint fracture from mechanical stress (vibration and shock) as well as from thermal stress (mismatch induced fatigue). The temperature range and added temperature range margin used in the analysis shall be defined in the final report. Any applicable part clamps or staking shall also be addressed. Flight production shall not proceed until the mechanical design analysis is reviewed and approved by the GSFC project PDL.

***Reliability Note 4.3:*** Polyimide boards are preferred when using CCGA packages, due to their lower CTE when compared to epoxy-glass boards.

### 4.3.2 Board Flatness

Board bow and twist shall be controlled in accordance with IPC-6012, Paragraph 3.4.3 and Appendix A, Class 3/A exception requirement (0.50% maximum for bow and twist). Each board shall be measured for flatness within the CCGA grid, to be ±0.003 in or ±0.3% across the longest dimension of the CCGA pad location using IPC-TM-650, 2.4.22 to verify this requirement is met. This requirement may be imposed via process specification and verified by supplier measurement.

### 4.3.3 Solder Surface Finish

Solder pads shall have a tin-lead solder or electroless nickel immersion gold (ENIG) finish. Pure tin or other lead free surface plating is not allowed without GSFC project approval.

***Reliability Note 4.4a:*** Reliability test data is not widely available for CCGA solder joints with electroless nickel immersion gold (ENIG) board surface plating. ENIG is allowed as long as the gold barrier layer thickness is controlled to less than 0.254 µm (see IPC J-STD-001DS.1, Paragraph 3.9.3). Controls on the thickness of the gold through purchase order requirements as well as quality assurance coupon inspection, shall be used to assure no danger of gold embrittlement in the finished solder joints.

***Reliability Note 4.4b:*** NPD 8730.2, NASA Parts Policy, requires GSFC projects to establish a lead-free control plan for all uses of lead-free platings in space flight hardware.

### 4.3.4 Pad Diameter

The pad diameter shall comply with the part supplier's recommendations or a minimum of 120% of the column diameter in the absence of the part supplier's specification. The pad diameter minimum size requirement provides for placement margin and sufficient area for solder deposition.

***Reliability Note 4.5:*** As column count increases and pitch gets tighter, the space under the CCGA can become very crowded when the "dogbone" pad-via design is used. Though thicker boards improve structural integrity, they can drive up via size due to aspect ratio manufacturing limitations. A filled via-in-pad approach may need to be considered to allow for sufficient pad size on thicker boards however solder joint voiding has been associated with this design approach.

### 4.3.5 Solder Mask

Solder mask design shall provide for non-solder mask defined (NSMD) pads. The solder mask edge shall not lie inside of the solder pad to prevent the edge of the solder mask from creating a stress point in the solder "joint".

***Reliability Note 4.6:*** Solder mask is required to prevent solder scavenging and insufficient joints caused by solder migrating down traces and into connected vias.

### 4.3.6 Vias

Vias shall not be shared at CCGA locations.

### 4.3.7 CCGA Placement Clearance (in the layout)

Parts surrounding each CCGA package shall be spaced to allow a minimum clearance of 0.3 inches around the CCGA package to allow for subsequent rework. Part mirroring shall require review and approval by the GSFC project.

***Reliability Note 4.7a:*** Part mirroring (a CCGA part located on one side of the board directly opposite another CCGA part on the other side of the board) is not recommended due to the combined effect the parts will have on the displacement behavior of the board, at that location, which may cause solder joint failure.

***Reliability Note 4.7b:*** The mechanical analysis will provide insight into "keep out" locations for CCGA attachments based on board vibration node points and maximum displacement transition regions.

### 4.3.8 Mechanical Part Retention

Mechanical retention of CCGA packages such as corner staking or corner brackets shall be based on successful qualification testing and shall be detailed on the assembly drawing.

### 4.3.9 PWB Design Review

The GSFC project shall conduct a peer design review of PWB designs containing CCGA patterns. Compliance with the requirements in this section shall be verified as a minimum as well as trades made where manufacturer recommended features could not be accommodated.

## 4.4 MANUFACTURING PROCESS PARAMETERS

### 4.4.1 Applicability of NASA-STD-8739.2 Requirements

Though NASA-STD-8739.2, Workmanship Standard for Surface Mount Technology, does not provide the requirements shown herein for CCGA interconnects, this does not relieve the supplier from meeting other applicable requirements, including:

a. Solder testing
b. Board cleaning and demoisturizing
c. Flux approvals
d. Soldering by certified personnel
e. Inspections by certified personnel

### 4.4.2 Underfill

Underfill shall not be used under CCGA packages.

### 4.4.3 Solder Volume

Solder volume shall be determined through engineering process development, and shall be a process/quality control parameter to result in uniform column wetting and solder fillets. Visual inspections shall be done for all deposited solder paste to verify uniformity, pad coverage, and to check for misplaced solder. Assemblers of boards with CCGA packages shall demonstrate the ability to verify solder paste volume. Solder paste placement shall be visually verified under magnification for 100% of the pads.

***Reliability Note 4.8a:*** Laser cut solder stencils have been found to be more effective in precisely controlling solder paste thickness than chemically etched stencils.

***Reliability Note 4.8b:*** Solder volume for reliable CCGA joints tends to be greater than the solder volume used for fine pitch traditional surface mount joints, because the column wicks more solder away from the joint area. Care shall be taken to ensure that excessive solder is not allowed to stiffen the column, thus reducing its reliability.

### 4.4.4 Part Placement (into the solder, prior to reflow)

Every CCGA package placed shall be visually verified to ensure part placement and polarity. Alternate methods for assuring accurate placement of CCGA parts prior to solder reflow shall be reviewed and approved by the GSFC project.

### 4.4.5 Reflow Profile

Reflow profile is critical and shall be designed, verified and controlled in accordance with the following requirements:

#### 4.4.5.1 Reflow Profile Design

A development board with a thermal capacity comparable to the flight unit with flight like mechanical CCGA package samples shall be used to develop an appropriate reflow profile. The inspection criteria of Section 4.4.10, Inspection Methods, shall be used to verify the profile design. Validation testing is recommended to assure the reflow profile design (see Section 4.6, Process Control Validation Testing).

#### 4.4.5.2 Temperature Quality Control

Temperature validation data is required prior to each reflow operation using a process validation unit. For multi-zone reflow systems, all temperature zones shall be instrumented at the board location where the board arrives at the middle of the zone, as a minimum. Acceptable temperature variation for each zone shall be defined. Temperatures shall be continuously monitored and recorded during processing of flight hardware. For single zone systems, such as localized hot air systems and rework systems, continuous temperature monitoring and recording are required. Hot air rework systems shall have the capability to quantitatively collect profile data, and rework processing should use a reflow profile as close as possible to the original profile.

***Reliability Note 4.9:*** The first cool down period after the solder has melted is the most critical for obtaining stress-free, undisturbed joints at the top and the bottom of the column.

### 4.4.6 Post-Soldering Cleaning

Cleaning requirements shall be in accordance with NASA-STD-8739.2.

### 4.4.7 Post-Soldering Inspection

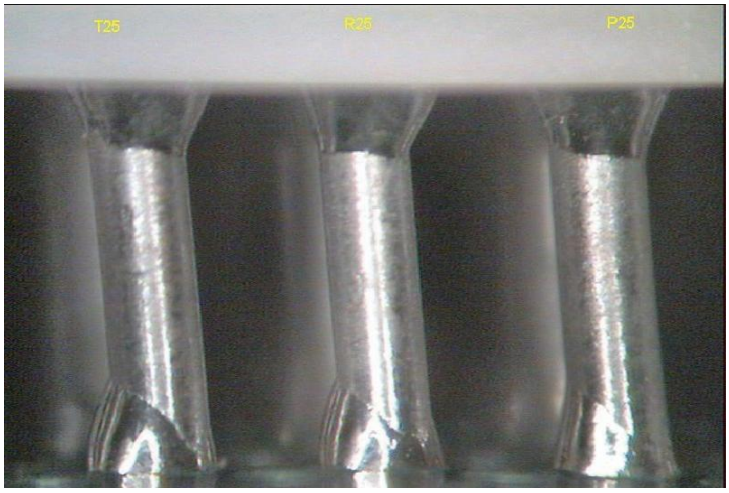
The inspection of the CCGA solder joints shall meet all applicable requirements of NASA-STD-8739.2 and the following:

#### 4.4.7.1 Visual Inspection of Outer Column Solder Joints

Visual inspection of all outer row CCGA solder joints (top and bottom) shall be performed at 10x magnification using the follow criteria:

a. NASA-STD-8739.2, Paragraphs 12.8.2. (b) (1) through 12.8.2(b)(15).
b. Solder fillet is present 75% around the circumference of the column
c. For columns made with solder dipped copper wrap (Six Sigma), there shall be no dewetting or absence of solder coverage on the column
d. Individual columns shall not be bent more than 5 degrees relative to other columns
e. All of the columns may be tilted uniformly up to 10 degrees and be acceptable as in figure 1. (Tilt is only acceptable if all columns are tilted uniformly).

f. Solder quality is shiny and does not indicate any cold solder joints. Inner pins shall also be inspected for these criteria, to the greatest extent possible




*Courtesy: ECSS Secretariat, ESA-ESTEC, ECSS-Q-70-38A*

**Figure 1 Example of acceptable column tilt up to 10 degrees.**

### 4.4.7.2 Radiographic Inspection (X-ray)

All columns shall be inspected using radiographic methods to screen for workmanship defects. X-ray equipment shall allow the operator to view the assembled PWA at a tilt, such that each individual column can be inspected, including the solder joints at the part and board sides (refer to Figure 2). Solder joints, with voids that appear to reduce the solder joint area by greater than 25%, require review and approval by the GSFC project via its MRB process prior to its use. Solder bridging or metallic/conductive contamination in the CCGA area shall be cause for rejection.

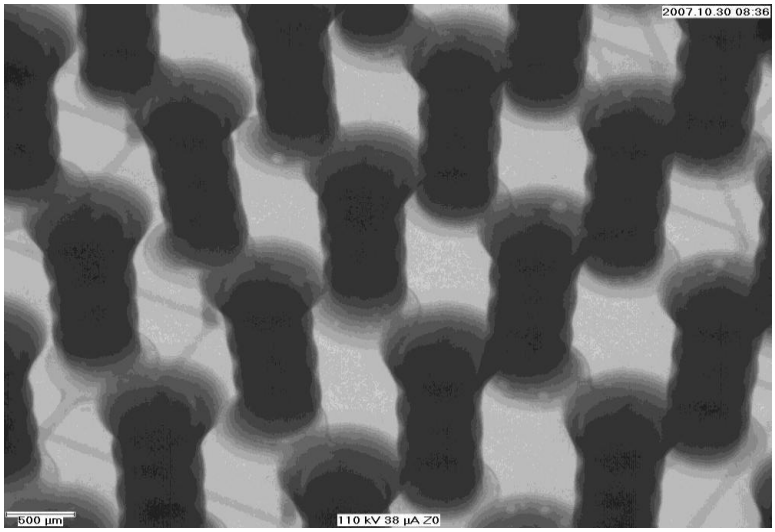



**Figure 2. Example of a Tilted X-ray View Showing an Acceptable Level of Voiding in the Solder Joints**

### 4.4.8 Staking

Staking shall not contact solder joints or any of the columns. Staking shall meet all applicable quality requirements of NASA-STD-8739.1A.

### 4.4.9 Conformal Coating

Conformal coating of boards with CCGAs shall follow the requirements of NASA-STD-8739.1A.

***Reliability Note 4.10:*** When the CCGA package contains a field programmable gate array it may be useful to mask the CCGA part during conformal coating until it is known to be the final design and then to add the coating later.

### 4.4.10 Inspection Methods

A summary of the inspection requirements is provided in Table 2.

**Table 2. Inspection Requirements Summary**

| Inspection Point and Inspection | Description | Section Reference |
|---|---|---|
| CCGA Incoming Inspection:<br>As-received part | Perform inspections at 10X magnification minimum.<br>Verify package-to-column solder joint quality.<br>Verify column quality.<br>Verify column alignment and coplanarity. | 4.2.3<br>4.2.3<br>4.2.3<br>4.2.4 |
| PWB Incoming Inspection:<br>Board flatness (bow and twist) | Perform 100% solder mask and pad area inspection within the CCGA package pattern.<br><br>Verify board flatness (bow and twist). | 4.2.5, 4.2.6, & 4.3.5<br>4.3.2 |
| Soldering Preparation:<br>Solder paste volume and placement | Verify solder paste volume.<br>Verify solder paste placement for 100% of the pads.<br>Visually inspect all deposited solder paste to verify uniformity, pad coverage, and to check for misplaced solder. | 4.4.3<br>4.4.3<br>4.4.3 |
| Soldering Preparation:<br>Part placement | Verify part placement and polarity of each CCGA package. | 4.4.4 |
| Workmanship Inspection, Soldering:<br>Solder joints | Perform visual inspection of outer solder joints.<br>Perform 100% Radiographic inspection of all joints for voiding, bridging, solder balls and metallic contamination. | 4.4.7<br>4.4.7.1<br>4.4.7.2 |
| Workmanship Inspection, Polymeric Applications: Staking and conformal coating | Perform visual inspection for requirements in NASA-STD-8739.1A, with Change 1, Paragraphs 6.7, and 13.5. | 4.4.8 & 4.4.9 |

## 4.5 Part Removal and Replacement

Part removal and replacement processes shall be documented and demonstrated in advance to verify the supplier's ability to rework CCGAs without causing part or board damage. Columns shall not be reused even if they remain attached to the part after part removal from the board and appear acceptable. The CCGA area of the board, at a minimum, shall be visually inspected for damage, solder mask damage, pad/trace damage, and cleanliness, after CCGA removal and pad redressing, prior to the installation of a new part. Newly applied solder paste shall also be inspected prior to the installation of a new part. In

addition, the newly placed replacement part shall be inspected for proper placement and polarity prior to the reflow operation. Final inspection of the reflowed CCGA shall be in accordance with Section 4.4.7, Post-Soldering Inspection. More than one part replacement at a single printed circuit board location may be damaging to the board and shall be treated as a repair. Repairs require prior review and approval in accordance with the GSFC project's PR/PFR process prior to implementation.

## 4.6 Process Control Validation Testing

Soldering process validation testing shall be required to demonstrate that the supplier's method of attachment is capable of meeting a baseline reliability standard. A recommended process validation test flow is detailed in Table 3; however, the actual test flow to be used shall be reviewed and approved by the GSFC project to confirm that it satisfies this requirement for process validation. This validation testing shows process capability and is intended to provide confidence to users that the process is a good candidate for use for flight hardware. Process control validation testing is not qualification testing (See Section 4.7, Qualification Testing).

***Reliability Note 4.11:*** The baseline reliability standard is defined by the industry standard test conditions for eutectic solder and solder column attachments defined herein (see Table 3).

No failures are permitted for the process control validation test board. Failures occurring prior to completion of the tests shall be submitted to root cause analysis. The minimum process validation test flow is detailed in Table 3. Processing of flight boards shall not commence until the results of the process validation testing are reviewed and approved by the GSFC project PDL and QA.

## 4.7 Qualification Testing

A board level qualification basis shall be established by the supplier and reviewed and approved by the GSFC project. If available, prior qualification data shall be submitted to the GSFC project for review and approval. If prior qualification data is not available, a Qualification Test Plan (QTP) shall be prepared by the supplier and submitted to the GSFC project for review and approval.

**Table 3. Process Validation Testing**

| Test | Conditions |
|---|---|
| Visual Inspection | The interconnects on the test board shall have met all visual and radiographic inspection criteria as defined in Sections 4.4.7, Post-Soldering Inspection, 4.4.7.1, Visual Inspection of Outer Column Solder Joints, 4.4.7.2, Radiographic Inspection (X-ray), and 4.4.10, Inspection Methods (refer to Table 2, Inspection Requirements Summary). |
| Electrical Baseline | Electrical continuity testing shall be performed to baseline a known good pre-test condition. |
| Vibration, Variable Frequency | MIL-STD-883, Method 2007, Condition A (20Gs peak acceleration) |
| Electrical Continuity | Perform electrical continuity testing of the daisy chained connections at -55º, + 100ºC and 25ºC to identify a failed attachment (1) |
| Thermal Cycling with Active Electrical Monitoring | Per IPC-9701, Paragraph 4.3 and Table 4-1, preconditioning applies. Temperature range shall be -55ºC to 100ºC(1), 200 cycles. Active monitoring during the last 10 cycles as a minimum is required. See IPC-9701 Table 4-4 for electrical failure criteria. Thermocouple monitoring of the package, the board, and the test chamber, is required. |
| DPA | At least one CCGA shall be cross-sectioned through an edge and center row. Buried vias and vias-in-pad shall be examined in cross-section. |

Note 1: Extreme temperatures for electrical tests are chosen to facilitate detection of cracks

# APPENDIX A

## TECHNOLOGY BACKGROUND

Ceramic Column Grid Array (CCGA) packages, as seen in Figure A-1, are being employed for high input/output (I/O) devices to enable short signal paths from the board to the semiconductor junction and to provide ultra-small device footprints. CCGA pins, though surface mount by type, are quite different in construction and thermo mechanical behavior than traditional surface mount leads on flat pack packages. As a result, design practices, manufacturing process techniques, inspection criteria, and qualification test methods will be different for these devices than those that are used for traditional surface mount devices (e.g. NASA-STD-8739.2). The standards invoked by NASA for workmanship (NASA Standards or IPC Standards) do not currently include requirements specific to column grid array interconnects.

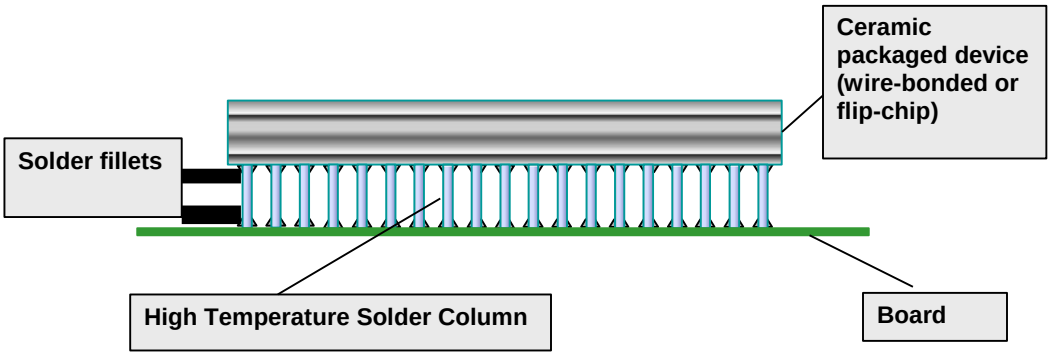



**Figure A-1. Elements of a CCGA Package**

Through evaluation testing and limited use by NASA, many aspects of the design and behavior of CCGA parts in flight application conditions are known, and design, manufacturing, and assurance rules can be defined and applied.

CCGA interconnect attach is normally associated with hermetic, ceramic packages. Originally, the under-package, high-density interconnect approach for ceramic packages began with through-hole pins in a pin grid array. Use of surface mount technology and high-speed performance needs drove interconnect designers to develop a ball grid array (BGA) attach for lightweight non-hermetic packages (plastic ball grid array or PBGA) which could closely match the very dense flip chip pin outs used inside the package. PBGA technology does not transfer to ceramic packages well because the various coefficients of thermal expansion of the ceramic, solder, and board can create excessive stress on the solder ball interconnects. When using ceramic packages, column grid arrays are a more reliable choice than ball grid arrays, because of the increased standoff height (distance between board and package) reduces fatigue on interconnects.

Generally columns have high melt-temperature solder with or without copper wrap reinforcement (see Figures A-2 and A-3). The ceramic package without the columns attached is

called a land grid array (LGA) package and has solder bumps which can be used for BGA or CCGA attach.

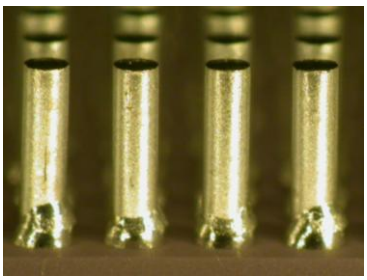


**Figure A-2. High-melt Temperature Solder Columns**

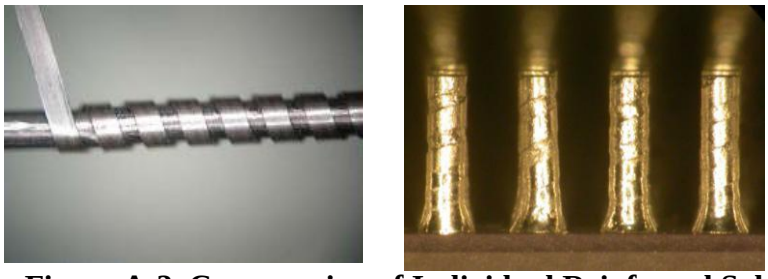


**Figure A-3. Construction of Individual Reinforced Solder Columns (left) and Finished Array (right)**

The primary reliability concern for these packages is fatigue on the solder joints due to thermal cycling and coefficients of thermal expansion (CTE) mismatches between the assembly materials. The heat generated by the operating device, such as a Field Programmable Gate Array (FPGA), coupled with the extreme thermal and mechanical conditions due to space flight, can cause a large temperature differential between the device and the board. This T coupled with large differences in the CTE among the interfacing materials used in the assembly will increase the stress, per cycle, on the joint (refer to Table A-1). Ultimately, excessive board displacements during periods of shock and vibration can create stress that exceeds the fracture strength of the solder or the column.

**Table A-1. Approximate CTEs of Materials Commonly Used in a CCGA Attached Assembly**

| Assembly Component | Material | CTE (ppm/°C) |
|---|---|---|
| Die/Chip | Si | 2.6 |
| Ceramic Substrate | $Al_2O_3$ | 7 |
| Solder | Pb/Sn | ~25 |
| Board | Polyimide | 12 - 16 |
| Board | FR4 | 14 - 20 |
| Board | Stablcor | 9-12 |

Problems that can result from a poorly designed board or poorly controlled assembly processes include voiding in the solder joints, bent pins from mishandling, misalignment of the CCGA, incomplete solder wetting, lack of solder fillet, and solder shorts between the columns. Also, the arrays can be very large (over 1000 pins) which makes many of the solder joints hidden and impossible to inspect using conventional methods. It is normally easy to visually find some defects in the outer row of the array, but workmanship defects which reside in the center of the array cannot be observed without radiographic inspection. An effective workmanship evaluation requires capable tools, experienced operators, and knowledge of the limitations of these inspection techniques.

Many of the advanced technology die which are being packaged in CCGA packages have been found in the past to also be very sensitive to electrostatic discharges (ESD); down to the most sensitive levels that have been defined (Class 0). Handling during all stages of part processing and installation onto boards should be performed only in areas in which ESD protections have been put into place and maintained. Attention should be given to the most applicable ESD event model relative to human and/or machine handling when assuring ESD workspace protections.